AMENDMENTS TO THE CLAIMS:

Please amend the claims as follows:

1-10. (Cancelled)

11. (Currently amended) A semiconductor device comprising:

a semiconductor wiring substrate, said semiconductor wiring substrate being composed of a semiconductor material, having a wiring layer;

a plurality of chip IPs mounted on said semiconductor wiring substrate by being bonded thereto;

a boundary scan test circuit provided in each of said chip IPs;

an internal scan chain for an internal scan test provided in each of said chip IPs,

a logic circuit which is a test object (DUT) in said chip IPs to be tested by said internal scan test; and

wherein the boundary scan test circuit and the internal scan chain for an internal scan test are formed so as to be capable of performing ~~a boundary scan test and~~ an internal scan test simultaneously with each other for testing said test object (DUT), using test data for an internal scan test which is input from outside, and

the boundary scan test circuit performs a boundary scan test in a boundary scan test mode and an internal scan test in an internal scan test mode.

12. (Original) The semiconductor device according to claim 11, wherein at least one of scanning signal input terminals connected to said internal scan chain is a terminal specially formed separately from said boundary scan test circuit.

13. (Original) The semiconductor device according to claim 11, wherein each of in-chip chains in said boundary scan test circuit of said plurality of chip IPs is formed so as to also function as said internal scan chain in the chip IP;

wherein an input-side wiring branch and an output-side wiring branch which respectively branch off from an input-side end portion and an output-side end portion of said boundary scan test circuit are formed in each of said chip IPs;

wherein a scan-in terminal of said internal scan chain is connected to said input-side wiring branch, while a scan-out terminal of said internal scan chain is connected to said output-side wiring branch; and

wherein an input to said in-chip chain can be selected from a signal in said boundary scan test circuit and a signal from said input-side wiring branch.

14. (Previously presented) A semiconductor device comprising:

a semiconductor wiring substrate, said semiconductor wiring substrate being composed of a semiconductor material, having a wiring layer;

a plurality of chip IPs mounted on said semiconductor wiring substrate by being bonded thereto;

a boundary scan test circuit provided in each of said chip IPs;

at least two pieces of wiring being formed in the wiring layer of said semiconductor wiring substrate to be used for testing only;

an input terminal and an output terminal, each connected to a different one of said chip IPs, for a boundary scan test connected to said boundary scan test circuit in each of said chip IPs and respectively connected to said two pieces of wiring for testing only; and

in addition to said input terminal and said output terminal, a scan-in terminal for inputting test data for an internal scan test directly from said at least two pieces of wiring to said boundary scan test circuit of at least one of said chip IPs, and a scan-out terminal for outputting a test result of an internal scan test directly to outside from said boundary scan test circuit of at least one of said chip IPs.

15. (Previously presented) The semiconductor device according to claim 14, wherein said boundary scan test circuit in said plurality of chip IPs is formed so as to also function as an internal scan test circuit in said chip IPs:

wherein in addition to said input terminal and said output terminal, an input-side wiring branch and an output-side wiring branch which respectively branch off from an input-side end portion and an output-side end portion of said boundary scan test circuit are formed in each of said chip IPs, and said input-side wiring branch is for inputting the test data for an internal scan test directly from outside and said output-side wiring branch is for outputting the test result of an internal scan test directly to outside;

wherein a scan-in terminal through which an internal scan test signal is input is connected to said input-side wiring branch;

wherein a scan-out terminal through which a scan test result is output is connected to said output-side wiring branch; and

wherein an input to an in-chip chain in said boundary scan test circuit can be selected from a signal in said boundary scan test circuit and a signal from said input-side wiring branch.

16. (Original) The semiconductor device according to claim 11, wherein said boundary scan test circuit in said plurality of chip IPs is formed integrally with said internal scan chain;

wherein said semiconductor device further comprises first special-purpose wiring which is formed in the wiring layer of said semiconductor wiring substrate, and through which a control signal is supplied to said internal scan chain in each of said chip IPs, and second special-purpose wiring which is formed in the wiring layer of said semiconductor wiring substrate, and through which signal in said internal scan chain in each of said chip IPs is output;

wherein a scan-in terminal of said internal scan chain in each of said chip IPs is connected to said first special-purpose wiring; and

wherein a scan-out terminal of said internal scan chain in each of said chip IPs is connected to said second special-purpose wiring.

17. (Withdrawn) A method for testing a semiconductor device including a logic circuit having a boundary scan test function and a built-in self-test (BIST) function, said method comprising: combining a built-in logic block observer (BILBO) function with the boundary scan test function of the logic circuit; and making a boundary scan test and a built-in self-test (BIST) on the logic circuit.

18. (Withdrawn) A method for testing a semiconductor device including a logic circuit having a boundary scan test function and a built-in self-test (BIST) function, said method comprising: providing a built-in logic block observer (BILBO) function in the logic circuit; and making a boundary scan test and a BIST on the logic circuit by supplying a linear feedback shift register (LFSR) signal as a boundary scan test signal to the logic circuit and by compressing boundary scan test results.

19-30. (Cancelled)